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EXAMINER	
VO, THANH DUC	
ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 10/680,170	**Applicant(s)** TENG, TOM
	Examiner Thanh D. Vo	**Art Unit** 2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 October 2005_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-53_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-6,11-16,20-31,36-41,46-48 and 50-53_ is/are rejected.

7)☒ Claim(s) _7-10,17-19,32-35,42-45 and 53_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _08 October 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Application filed on October 8, 2003. Claims 1-53 are presented for examination. Claims 1-53 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on January 7, 2004 was filed after the mailing date of the application on October 8, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 50 recites the limitation "the number of row per bank", "the selected parameter", and "the command stream" in page 27. There is insufficient antecedent basis for this limitation in the claim.

4. Claims 20 and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 discloses a first status register field for storing row address information. Further review indicates that status register is to store the status information wherein claim 20 discloses the status register to store the row address information. There is an obvious contradiction of disclosure in claim 20 and therefore it is indefinite.

Claims 53 is being indefinite since it fails to particularly point out if the smallest parameter is of the maximum refresh interval in compare with the maximum parity-scan interval or the smallest parameter of maximum refresh interval and the smallest parameter of maximum parity-scan interval.

The following phrases from claim 53 are also indefinite:

1) generating command, enable and address values

2) selecting a value indicative of the operation to be performed. The indicative value is being indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 11-16, 20-31, 36-41, 46-48, and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batson et al. (hereinafter “Batson”) of U.S. Patent 6,760,881 further in view of Srinivasan et al. (hereinafter “Srinivasan”) of U.S. Patent 6,678,786.

5. As per claims 1, 11, 26, 36, and 48 Batson discloses a processor system comprising:

a processor (in claims 26, 36, and 48) is an inheritance feature in the computer art since a processor is required in order to process information and command; and

a memory device (See col. 2, line 15) coupled to said processor, said memory device comprising a circuit for coordinating refresh and parity-scan operations in said memory device (See col. 2, lines 12-18, wherein parity-scan operation is equivalent to parity validation), said circuit comprising:

a plurality of memory cells organized as an array of rows and columns (See col. 1, lines 25-37, wherein array of CAM cells are organized in row and column) *with respect to claims 11 and 36*;

control logic coupled to the register fields for coordinating refresh and parity-scan operations on the memory cells, said control logic using the information in the register fields to schedule parity-scan operations as a substitute for refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations (See col. 3, line 34 – col. 4, line 12 and Fig. 2a-b). Furthermore, control logic is an inheritance feature in memory refresh and parity validation in order to determine and coordinately operate said operations. Figures 2a-b also clearly disclosed the control logic which coordinate the operations on the memory cells. And the parity validation (col. 3, line 40) is assigned to substitute the refresh operation as it determined to be substitutable.

Batson failed to disclose "a plurality of register fields, said register fields containing information regarding the memory device" as apply to all claims.

Srinivasan discloses a plurality of register fields, said register fields containing information regarding the memory device. See col. 4, lines 12-24.

Batson and Srinivasan are from the field of endeavor, which is computer memory especially both are concentrating in Content Addressable Memory device.

Therefore, it would have been obvious to a one having an ordinary skill in the art at the time of the Applicant's invention to combine the register fields disclosed in Srinivasan with the system of Batson.

The motivation of doing so is in order to to perform any comparison or control logic to carry out a result or an operation. In addition, Batson further disclosed "parity generator" and "exclusive OR logic tree" (col. 4, lines 3-12) wherein register fields are most useful to perform said operations.

Therefore, it would have been obvious to one having an ordinary skill in the memory art to modify the method of Batson to include register fields so that the information regarding to the states, flags, comparand, or data could easily stored in the registers to perform operations as disclosed in these claims.

As per claims 2, 12, 27, 37, Batson failed to explicitly disclose, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations. However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that once the parity-scan operations cannot be substitute for refresh operations then schedule for a refresh operations is old and well known method to fully cover various states of the parity checking and refresh operation in memory art. In doing so, the system will only operation the refresh operation once it is indicated that the parity-scan operation is not required. Since refresh operation is a single operation compare to parity-scan which comprise of read, refresh, and parity checking that requires more time and system resource. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Batson to include said method to arrive at the invention said forth.

As to claims 3, 13, 28, 38, Batson failed to disclose a plurality of register fields comprise **configuration register fields containing configuration information**.

Srinivasan disclosed the register field comprises configuration register fields containing configuration information. See col. 4, lines 12-24.

Batson and Srinivasan are from the field of endeavor, which is computer memory especially both are concentrating in Content Addressable Memory device.

Therefore, it would have been obvious to a one having an ordinary skill in the art at the time of the Applicant's invention to combine the configuration register fields disclosed in Srinivasan with the system of Batson.

The motivation of doing so is to use the configuration information to indicate the current states or comparand information that would be extremely useful in the memory control logic to perform the limitation disclosed in claims 1, 11, 26, 36, and 48.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Batson to include the configuration register field of Srinivasan to arrive at this claim invention.

As per claims 4, 14, 29, and 39, Batson failed to disclose, wherein said plurality of register fields further comprise command register fields containing command information.

However, command register field is old and well known in the computer art at the time of the Applicant's invention. Furthermore, a command is a required feature in the control logic and computer art in order to instruct the system as when and how to operate the system accordingly to avoid any system fault while enhancing the system timing.

Therefore, it would have been obvious to a one having an ordinary skill in the art at the time of the Applicant's invention to have the command register fields disclosed in the system of Batson.

As per claims 5, 15, 30, and 40, Batson failed to disclose, wherein said plurality of register fields further comprise status register fields containing status information.

Srinivasan disclosed a register field further comprises status register field containing status information. See col. 4, line 51 – col. 5, line 8.

Batson and Srinivasan are from the field of endeavor, which is computer memory especially both are concentrating in Content Addressable Memory device.

At the time of the Applicant's invention it would have been obvious to a one having an ordinary skill in the art to combine the status register fields disclosed in Srinivasan with the system of Batson.

The motivation of doing so is to indicate the system the status of an operation so that the control logic will determine a next proper operation that will be best suit for the current system condition with current status information.

Therefore, it would have been to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Batson to include the system of Srinivasan to arrive at the invention discloses in these claims.

As to claims 6, 16, 31, 41:

Claims 6, 16, 31, and 41 are the combination of the limitations that have been rejected in claims 3-5, 13-15, 28-30, and 38-40. Examiner respectfully request Applicants to refer to previously indicated claims for the manner of rejection.

As per claim 20, Batson further disclosed:

a first register field for storing row address information (see col. 1, lines 25-45); and

Batson failed to disclose a status register field for indicating that all rows have been scanned before the end of a scan period. However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that a status register indicating all rows have been scanned before the end of the scan period is old and well know technique in the computer art from software to hardware. Said status register will protect the system from running indefinitely when the scanning operation is activated. Therefore, it is obvious to one having an ordinary skill in the computer to combine the status register to indicate that all rows have been scanned to arrive at the invention claim in claim 20.

As per claims 21 and 46, Batson disclosed the memory device, wherein said memory cells are dynamic random access memory cells. See col. 1, lines 8-31.

As per claims 22 and 47, Batson disclosed the memory device, wherein said memory cells are content addressable memory cells comprised of dynamic random access memory. See col. 1, lines 8-31.

As per claim 23, Batson disclosed a memory device comprising:

means for substituting parity-scan operations on memory cells of the memory device for refresh operations. See col. 3, line 34 – col. 4, line 12 and Fig. 2a-b.

Batson failed to disclose "a plurality of register fields, said register fields containing information regarding the memory device" as apply to all claims. However, it would have been obvious to a one having an ordinary skill in the art at the time of the Applicant's invention to realize that register fields are old and well know in the computer art. Especially in the memory refreshing and parity checking field, where the register fields are widely used to store the flags, states, or data in order to perform any comparison or control logic to carry out a result or an operation. In addition, Batson further disclosed "parity generator" and "exclusive OR logic tree" (col. 4, lines 3-12) wherein register fields are most useful to perform said operations.

Therefore, it would have been obvious to one having an ordinary skill in the memory art to modify the method of Batson to include register fields so that the information regarding to the states, flags, comparand, or data could easily stored in the registers to perform operations as disclosed in these claims.

As per claim 24, Batson disclosed the memory device, wherein said memory cells are dynamic random access memory cells. See col. 1, lines 8-31.

As per claim 25, Batson disclosed the memory device, wherein said memory cells are content addressable memory cells comprised of dynamic random access memory. See col. 1, lines 8-31.

As per claim 50, Batson disclosed a method of coordinating refresh and parity-scanning in a memory array, comprising:

determining whether parity-scan operations can be substituted for refresh operations and scheduling the parity-scan operations when it is determined that the parity-scan operations can be substituted for refresh operations. (See col. 3, line 34 – col. 4, line 12 and Fig. 2a-b). Furthermore, figures 2a-b clearly disclosed the control logic which coordinate the operations on the memory cells. And the parity validation (col. 3, line 40) is assigned to substitute the refresh operation as it determined to be substitutable.

As per claims 51, Batson failed to explicitly disclose, wherein the claim 50 further comprising the step of scheduling refresh operations when it is determined that parity-scan operations cannot be substituted for refresh operations. However, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that once the parity-scan operations cannot be substitute for refresh operations then schedule for a refresh operations is old and well known method to fully cover various states of the parity checking and refresh operation in memory art. In doing so, the system will only operation the refresh operation once it is indicated that the parity-scan operation is not required. Since refresh operation is a single operation compare to parity-scan which comprise of read, refresh, and parity checking that requires more time and system resource. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Batson to include said method to arrive at the invention said forth.

As per claim 52, Batson further disclosed the step of checking parities returned from the memory array to ensure data integrity. See col. 4, lines 1-26.

6. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Batson et al. (U.S. Patent 6,760,881) and further in view of Batson et al. (U.S. Patent 6,430,073).

As per claim 49, Batson et al. ('881) disclosed memory device comprising:

means for substituting parity-scan operations on memory cells of the memory device for refresh operations. See col. 3, line 34 – col. 4, line 12 and Fig. 2a-b.

Batson et al. ('881) failed to disclose "a plurality of register fields, said register fields containing information regarding the memory device" as apply to all claims. However, it would have been obvious to a one having an ordinary skill in the art at the time of the Applicant's invention to realize that register fields are old and well know in the computer art. Especially in the memory refreshing and parity checking field, where the register fields are widely used to store the flags, states, or data in order to perform any comparison or control logic to carry out a result or an operation. In addition, Batson further disclosed "parity generator" and "exclusive OR logic tree" (col. 4, lines 3-12) wherein register fields are most useful to perform said operations.

Therefore, it would have been obvious to one having an ordinary skill in the memory art to modify the method of Batson to include register fields so that the information regarding to the states, flags, comparand, or data could easily stored in the registers to perform operations as disclosed in these claims.

Batson et al. ('881) failed to disclose a router.

Batson et al. ('073) disclosed a Network Router (col. 1, lines 11-17)

Both of the patents are from the same inventor and the same field of the endeavor, memory refreshing and parity checking.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to implement the invention of Batson et al. ('881) into the router disclosed by '073.

The motivation of doing so is make use of the content addressable memory in the router in order to accomplish the fastest searching of stored data in the memory that comprising refreshing and parity checking as disclosed by '073 col. 1, lines 15-17.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Batson et al. ('881) to combine with '073 to arrive at the invention claims in claim 49.

Allowable Subject Matter

7. Claims 7, 17, 32, and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 7, 17, 32, 42, while Batson disclosed the combination of refresh operation and parity-validation comprises of comparator, registers, and suggesting a coordinating logic to control the refresh and parity-validation logic but failed to disclosed:

a comparator comparing a maximum refresh interval with maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enable or disable by information within said registers; and

coordinating logic for using the information with the registers to control the self-refresh and parity-scan logic.

Examiner also further review the most relevant references that are in the memory device with parity checking, refreshing, and self-refreshing field of art but all has failed to overcome the combination of the limitations with respect to the present invention. Therefore, claims 7, 17, 32, and 42 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 8-10:

Claims 8, 9, and 10 would also be allowable since they are the dependent claims of claim 7.

As to claims 18 and 19:

Claims 18 and 19 would also be allowable since they are the dependent claims of claim 17.

As to claims 33-35:

Claims 33, 34, and 35 would also be allowable since they are the dependent claims of claim 32.

As to claims 43-45:

Claims 43, 44, and 45 would also be allowable since they are the dependent claims of claim 42.

8. Claim 53 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

As to claim 53, Batson further disclosed, wherein the determining step comprises:

tracking a next row to be refreshed or parity-scanned (see Fig. 2a-b and their respective descriptions in Specification). In addition, in the CAM memory art the device is continuously checking the memory cells that are needed to be refreshed or scanned.

generating command, enable and address values are inheritance feature in the memory cell refresh and parity checking since the control logic is known to require the command, register, signal lines including enabling and disabling to perform logic flawlessly.

However, Batson and related prior arts failed to disclose the following limitations:

selecting a smallest parameter between a maximum refresh interval and a maximum parity-scan interval;

dividing the smallest [[selected]] parameter by *the number of rows per bank* to generate a wrap-around limit;

sending an increment signal to a counter when said wrap-around limit is met;

selecting a value indicative of the operation to be performed; and

checking the command [[stream]] for idle cycles to insert parity-scan or refresh.

Therefore, claim 53 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims while overcoming the rejection(s) under 35 U.S.C 112, 2nc paragraph.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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TUAN V. THAI
PRIMARY EXAMINER